CLAIMS:

What is claimed is:

1. A method for managing a read request, comprising:

receiving, at a first controller, a read request for a data block;

allocating a memory buffer for the data block from a memory pool that includes a first memory on the first controller and a second memory on a second controller, wherein the memory buffer resides in the second memory;

retrieving the data block from a storage device; and

caching the data block in the memory buffer.

2. The method of claim 1, wherein the first controller includes a first switch and the second controller includes a second switch.

3. The method of claim 2, wherein the first switch and the second switch are coupled using a switch-to-switch path.

4. The method of claim 3, wherein the step of caching comprises storing the data block in the second memory via the switch-to-switch path.

5. The method of claim 3, wherein the step of retrieving the data block comprises retrieving the data block from the storage device using a drive adapter on the second controller via the switch-to-switch path.

6. The method of claim 2, wherein the step of retrieving the data block comprises retrieving the data block from the storage device using a drive adapter on the first controller via the first switch.

7. A method for managing a read request, comprising:

receiving, at a first controller, a read request for a data block; and

retrieving the data block from a memory pool that includes a first memory on the first controller and a second memory on a second controller, wherein the data block resides in the second memory.

8. The method of claim 7, wherein the first controller includes a first switch and the second controller includes a second switch.

9. The method of claim 8, wherein the first switch and the second switch are coupled using a switch-to-switch path.

10. The method of claim 9, wherein the step of retrieving the data block from the memory pool comprises retrieving the data block from the second memory using the switch-to-switch path.

11. A method for managing a write request, comprising:

receiving, at a first controller, a write request for a data block;

allocating a primary data buffer for the data block in a first memory and a mirror data buffer for the data block in a second memory, wherein the first memory resides on one of the first controller and a second controller and the second memory resides on the other of the first controller and the second controller;

storing write data for the data block in the primary data buffer; and

mirroring the write data in the mirror data buffer.

12. The method of claim 11, wherein the first controller includes a first switch and the second controller includes a second switch.

13. The method of claim 12, wherein the first switch and the second switch are coupled using a switch-to-switch path.

14. The method of claim 13, wherein the first memory resides on the second controller and the step of storing write data for the data block in the primary data buffer comprises storing the write data in the primary data buffer via the switch-to-switch path.

15. The method of claim 13, wherein the second memory resides on the second controller and the step of mirroring write data in the mirror data buffer comprises storing the write data in the mirror data buffer via the switch-to-switch path.

16. The method of claim 13, further comprising:

writing the write data to a storage device using a drive adapter on the second controller via the switch-to-switch path.

17. The method of claim 12, further comprising:

writing the write data to a storage device using a drive adapter on the first controller via the first switch.

18. An apparatus, in a first controller, comprising:

a host adapter that provides a connection to a host;

a processor;

a memory controller that manages a connection to a memory;

a drive adapter that provides a connection to a storage device;

a first switch that connects the host adapter, the processor, the memory controller, and the drive adapter; and

a switch-to-switch path that connects the first switch to a second switch on a second controller.

19. The apparatus of claim 18, wherein the host adapter receives a read request for a data block; and

wherein the processor allocates a memory buffer for the data block from a memory pool that includes a first memory on the first controller and a second memory on the second controller, wherein the memory buffer resides in the second memory; retrieves the data block from a storage device; and caches the data block in the memory buffer via the switch-to-switch path.

20. The apparatus of claim 19, wherein the processor retrieves the data block from the storage device using the drive adapter via the first switch.

21. The apparatus of claim 19, wherein the processor retrieves the data block from the storage device using a drive adapter on the second controller via the switch-to-switch path.

22. The apparatus of claim 18, wherein the host adapter receives a read request for a data block; and

wherein the processor retrieves the data block from a memory pool that includes a first memory on the first controller and a second memory on the second controller, wherein the data block resides in the second memory.

23. The apparatus of claim 18, wherein the host adapter receives a write request for a data block; and

wherein the processor allocates a primary data buffer for the data block in a first memory and a mirror data buffer for the data block in a second memory, wherein the first memory resides on one of the first controller and the second controller and the second memory resides on the other of the first controller and the second controller; stores write data for the data block in the primary data buffer; and mirrors the write data in the mirror data buffer.

24. The apparatus of claim 23, wherein the first memory resides on the second controller and the processor stores the write data in the primary data buffer via the switch-to-switch path.

25. The apparatus of claim 23, wherein the second memory resides on the second controller and the processor stores the write data in the mirror data buffer via the switch-to-switch path.

26. The apparatus of claim 23, wherein the processor writes the write data to a storage device using the drive adapter via the first switch.

27. The apparatus of claim 23, wherein the processor writes the write data to a storage device using a drive adapter on the second controller via the switch-to-switch path.